PVP 12

Code: **CSCS1T3**

I M.Tech-I Semester-Regular Examinations-April 2015

COMPUTER ORGANIZATION AND ARCHITECTURE

(COMPUTER SCIENCE & ENGINEERING)

Duration: 3 hours Marks: 5x14=70

Answer any FIVE questions. All questions carry equal marks

1 a) NOR and NAND gates are called universal gates. Justify the statement. 3 M

b) How do you perform subtraction using 2's complement method. 3 M

c) Perform the arithmetic operation (+42) + (-13) and (+42) - (-13) in binary using 2's complement subtraction. 8 M

2 a) Explain the operation of J-K flip flop with a neat sketch. 7 M

b) Design a full adder with NAND gates. 7 M

3 a) What is content addressable memory? Explain the operation with the help of a block diagram. 6 M

b) Derive the match logic for each word in associative memory and draw the logic diagram. 8 M

4 a) What are the functions performed by an I/O interface? 4 M

b) Explain the data transfer using hand shaking procedure between CPU and I/O devices. 10M

5 Write an algorithm for the multiplication of numbers represented in signed 2's Complement representation. Trace the algorithm with (-14) and (-23). 14 M

6 a) What is an instruction pipeline? Explain the operation of an instruction Pipeline with a flow chart and timing diagram. 10 M

b) Briefly explain various ways in which an instruction pipeline can deal with conditional branch instructions. 4M

7 a) Compare the characteristics of large register file and cache. 7 M

b) Write about compiler based register optimization and give an example. 7 M

8 a) What is MESI protocol? Explain the different states of MESI protocol and the transition diagram. 7 M

b) Write briefly about the Flynn's classification of computer systems with parallel processing capability. 7 M